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Published in:
2nd 6G Wireless Summit 2020

DOI:
10.1109/6GSUMMIT49458.2020.9083918

Published: 01/03/2020

Document Version
Publisher's final version

Link to publication

Please cite the original version:
Lamminen, A., Lahti, M., Del Rio, D., Saily, J., Sevillano, J. F., & Ermolov, V. (2020). Characterization of interconnects on multilayer high frequency PCB for D-band. In *2nd 6G Wireless Summit 2020: Gain Edge for the 6G Era, 6G SUMMIT 2020* [9083918] IEEE Institute of Electrical and Electronic Engineers. https://doi.org/10.1109/6GSUMMIT49458.2020.9083918

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Characterization of Interconnects on Multilayer High Frequency PCB for D-Band

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***Abstract*—The paper presents the characterization of interconnects for D-band on multilayer high frequency PCBs. The losses demonstrated at 150 GHz for a microstrip line, a coplanar waveguide and a single flip-chip transition are 1.9 dB/cm, 1.8 dB/cm and 0.3 dB (for 60 µm bumps), respectively. The applicability of multilayer high frequency PCB technology as a low cost integration platform for D-band is proven.**

Keywords—*integration, D-band, mm-waves, interconnect, flip-chip interconnect, PCB*

I. Introduction

The explosive growth of data traffic demands tens and even hundred Gbit/s backhaul capacities in future 5G and beyond 5G mobile networks [1]. It requires the usage of large bandwidths, which are available only in the high millimetre-wave and sub-terahertz regions [2], [3]. Free spectrum in D-band (130 to 175 GHz) offering a vast bandwidth is considered as a strong candidate for high capacity backhaul networks for 5G and beyond [3]. The level of integration of monolithic microwave integrated circuits (MMIC) has increased drastically in the last years. However, modern communication systems request sophisticated interconnection of many elements: MMICs, passive components and antennas. Thus, successful commercialization of D-band communication systems is not possible without advanced integration technologies providing size miniaturization, cost reduction and performance enhancement of the systems. Several packaging platforms have been demonstrated for D-band applications: low temperature co-fired ceramic (LTCC) [4], integrated passive device (IPD) [5] and thin-film processing on alumina substrate [6]. LTCC provides multilayer metal structures but it is not a cost-effective solution in large scales. IPD technology enables conductive layers inside polymer films on top of a carrier substrate but the layer thickness and the number of layers is usually limited. Thin-film processes usually have only a single patterned layer over a ground plane layer. Such process is not feasible for complex integrated systems like phased antenna arrays. Polytetrafluoroethylene (PTFE) -based substrates have been used in printed circuit boards (PCB) for low cost 77 GHz radars [7]. However, PTFE has low mechanical strength and is difficult to manufacture in multilayer substrates. Low-loss multilayer integration solutions have become available, for example based on LCP (Liquid Crystal Polymer) [8]. However, LCP suffers from inconsistent material movement that complicates the PCB fabrication process, particularly for mm-wave applications where feature-to-feature accuracy is a prime consideration. In recent years, new cost-effective and low-loss multilayer build-ups, which can be manufactured using PCB processing techniques, have entered the market [9].

Interconnects play a key role in any integration platform. They should have low loss and wide bandwidth. Transmission lines are needed in phased array feeding networks to distribute RF signals to all array elements. Flip-chip interconnects are needed to integrate the MMIC to PCB. In this work, the performance of microstrip lines (MS), coplanar waveguides (CPW) and flip-chip interconnects are studied on high frequency multilayer PCBs at D-band. A possible utilization of such interconnects for a physical implementation of a D-band transceiver with a phased antenna arrays is shown in Fig. 1.

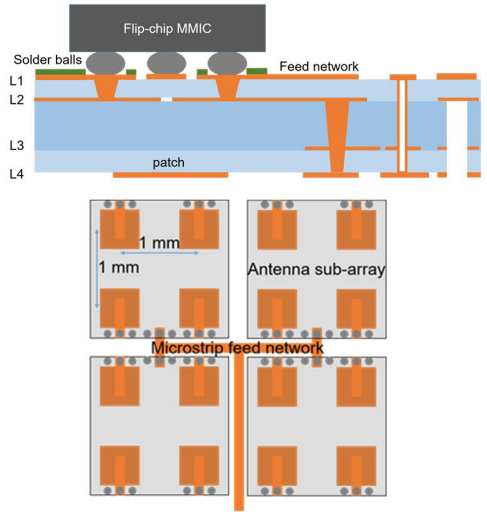

Fig. 1. Example of a physical implementation of D-band transceiver with an antenna array on high frequency PCB.

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 761390.

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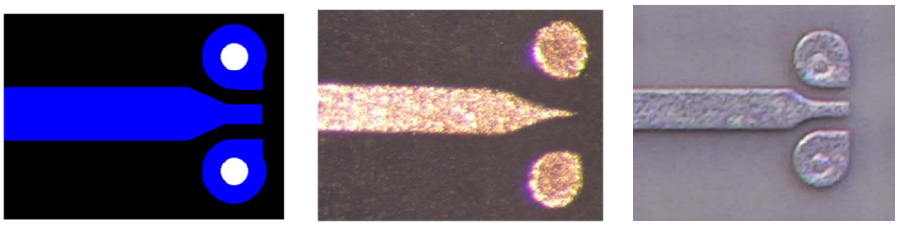
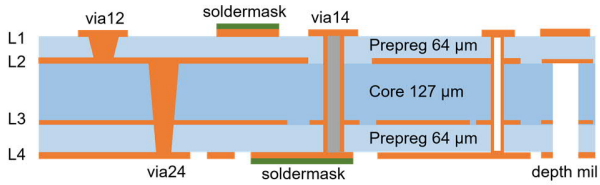


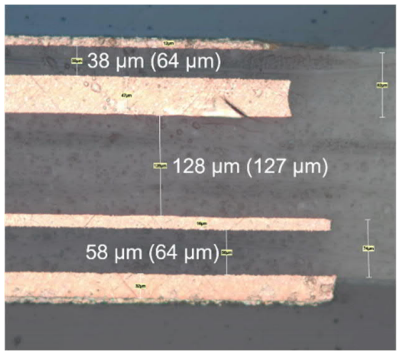
Fig. 3 (a) Layout and micrographs of a microstrip after (b) subtractive and (c) mSAP processing.

II. Fabrication of Interconnects

A 4-layer PCB build-up is selected for fabrication of interconnect test structures. The PCB build-up is shown in Fig. 2.



(a)



(b)

Fig. 2. (a) Schematic of PCB material build-up, (b) cross section of fabricated PCB (Astra® MT77 by Isola Group as substrate material and conventional subtractive technology for conductor patterning) with realized and designed dimensions (in brackets).

PCB test panels were ordered from two different PCB producers. The first producer use Astra® MT77 ($\varepsilon_r = 3.0 \pm 0.1$, $\tan\delta = 0.0015 \pm 0.0005$ up to 100 GHz) by Isola Group as substrate material and conventional subtractive technology for conductor patterning. In case of subtractive technology, conductive structures are formed by etching copper layers. The second producer use Megtron 7N ($\varepsilon_r = 3.20$, $\tan\delta = 0.003$ at 50 GHz) by Panasonic as substrate material and semi-additive processing (mSAP) for conductor patterning. The mSAP process starts with the deposition of a copper seed layer. Then a mold for plating the copper is created by photolithography. After the copper is plated to the desired thickness, the photoresist mold is stripped and the seed layer is removed to complete the metal layer. Laminate and pre-preg materials are available down to 50-µm and 60-µm thicknesses from both producers. Both material systems are designed for advanced multilayer constructions with sequential laminations, also called any-layer build-ups.

Microstrip lines (MS) and grounded coplanar waveguides (GCPW) were designed for PCBs to investigate their loss/cm and matching with the ground-signal-ground (GSG) pads that are used for flip-chipping. Due to close dielectric properties of Astra® MT77 and Megtron 7N, the same designs were used for both PCBs. The designed width of the 50 Ω MS is 140µm. The designed line and gap widths of the GCPW are 120µm and 70µm, respectively. The critical areas for fabrication are the ground-signal-ground (GSG) probe contact pads where track widths down to 50 µm and gap widths of 50 µm are required (see Fig. 3a).

After fabrication, the dimensions of GCPW and other transmission lines were measured under a microscope. Comparison between MS layout and manufactured MS can be seen in Fig. 3. The strong over-etching was observed for PCB using subtractive technology (see Fig. 3b). Deviations of dimensions was up to 12%. Especially, areas of contact pads were very strongly over-etched, making the structures barely usable. A cross section of PCB fabricated by the first producer is shown in Fig. 2b. The realized (designed) thicknesses of the top, middle, and bottom dielectric layers are 38µm (64 µm), 128 µm (127 µm), and 58 µm (64 µm), respectively. Since the feed line is on the top layer, the deviation affects mainly on the feed line impedance. Quality of metal patterning in case of mSAP processing was much better (see Fig. 3c). The realized dimensions are only about 2.5% smaller than the designed ones.

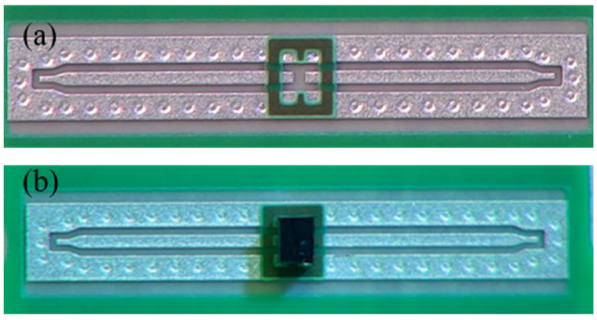


Fig. 4. (a) The coplanar waveguide on the PCB with contact pads for MMIC. A frame around pads is a soldering mask preventing the solder from flowing along copper tracks. (b) The test structure with the MMIC dummy chip attached.

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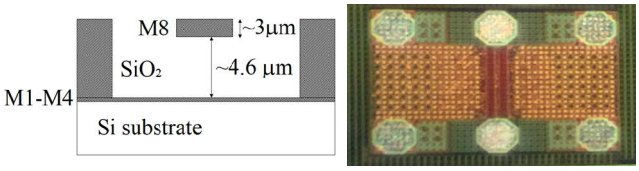

(a) (b)

Fig. 5. (a) Cross-section diagram of the on-chip transmission line and (b) micrograph of the manufactured on-chip transmission line.

To demonstrate the flip-chip interconnects, prototypes were fabricated that consist of two parts: a GCPW with bond pads fabricated on PCB (see Fig. 4a) and a SiGe MMIC test chip with a 50 Ω transmission line and bond pads. For the on-chip test structure, a side-shielded microstrip line is implemented using the 55-nm BiCMOS process from STMicroelectronics [10]. With 8 metal layers, including an ultra-thick layer with a thickness of around 3 µm, as well as heterojunction bipolar transistors (HBT) with f_t higher than 300 GHz, this technology has a strong potential to allow the implementation of high-performance D-band circuits [11], [12].

The main conductor of the transmission line is implemented using the 8th ultra-thick metal, while the first four metals are stacked to provide a low-resistivity return plane. Fig. 5a shows a simplified diagram of the transmission line cross section. The line has a width of 5.4 µm to present a characteristic impedance of 50 Ω at 150 GHz, its length is 135 µm and the separation to the side ground walls is 13.5 µm. This line provides a simulated insertion loss of 0.9 dB/mm at 150 GHz. For the interconnections, custom octagonal GSG pads are implemented, with a diameter of 60 µm and a pitch of 150 µm. Special care is placed in the transition from the on-chip microstrip line to the coplanar pads, so as to maximize the return loss. A picture of the part of the manufactured test chip that includes the described transmission line is shown in Fig. 5b. After dicing out this part of the chip, it has a size of 0.420 mm × 0.320 mm and total thickness is 300 µm.

Fig. 6 depicts the EM simulated S-parameters of the transmission line, including the GSG pads. As observed, the total insertion loss at 150 GHz is 1.4 dB, of which around 0.6 dB are due to each group of GSG pads and CPW-microstrip transition.

60 um solder bumps were processed on the chips. The chip is flip-chipped to the coplanar waveguide on the PCB. Due to strong over-etching of subtractive processed PCB only mSAP processed PCB were used for characterization of flip-chip interconnects. In the assembly process, solder flux was first dispensed onto the pads of the chip. The chip was then aligned on the correct location using the Finetech Fineplacer flip-chip bonder.

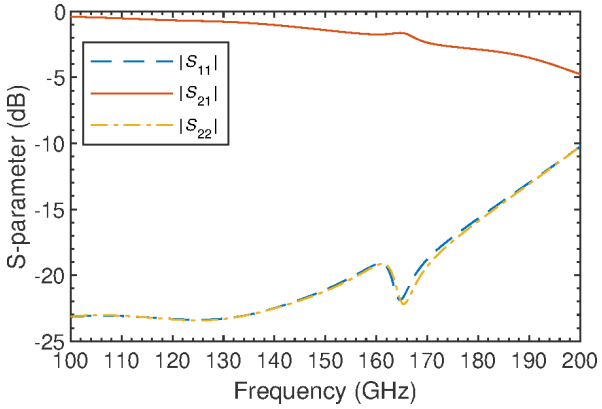

Fig. 6. EM simulation results of the on-chip transmission line.

The placement accuracy was about a few µm. One of the benefits of soldering over thermo-compression bonding is the self-alignment of the chip during soldering. Reflow soldering was carried out in Sikama Falcon 5C belt oven. The peak temperature was 245 °C to ensure the melting of SnAgCu solder bumps. The test structure with the MMIC dummy chip attached is shown in Fig. 4b.

III. Results and Discussion

A. Transmission lines

The S-parameters of the test structures were measured at D-band (110–170 GHz) using PNA-X N5245A with WR6.5-VNAX extenders and ground-signal-ground (GSG) probes with 100-µm pitch. The line-reflect-reflect-match (LRRM) calibration method is used in the measurements, thus the GSG transition needed for the probes presents in the results.

The measured S-parameters for the 10 mm long MS and GCPW on PCB using Astra® MT77 by Isola Group as substrate material and conventional subtractive technology for conductor patterning are presented in Fig. 7. It can be seen that $|S_{11}|$ increases with frequency due to the GSG transition. By excluding the mismatch of the GSG transitions, the measured losses for the MS and GCPW are 2.6 dB/cm and 2.9 dB/cm, respectively, at 150 GHz, which are higher than for ideal copper (0.92 dB/cm and 0.83 dB/cm). The difference is mostly due to surface roughness of the conductors which can be taken into account in simulations by using effective conductivity (σ_{eff}) instead of bulk value. Re-simulations were done to match the simulation results with the measured ones. Good agreement was observed with parameters $\varepsilon_r = 3.00$, $\tan\delta = 0.0017$ and $\sigma_{eff} = 3\times10^6$ S/m for the conductors.

The measured S-parameters for the 10 mm long MS and GSG on PCB using Megtron 7N by Panasonic as substrate material and semi-additive processing (mSAP) for conductor patterning are presented in Fig. 8. The insertion losses are lower than for the subtractive technology in Fig. 7.

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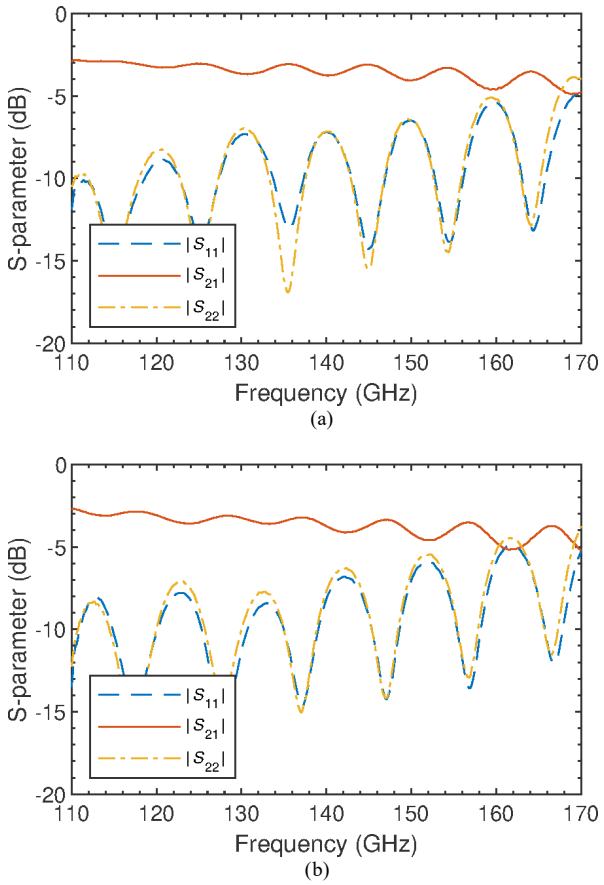

Fig. 7. Measured S-parameters (LRRM calibration) for the 10 mm long (a) microstrip line and (b) coplanar waveguide on PCB using Astra® MT77 by Isola Group as substrate material and the subtractive technology.

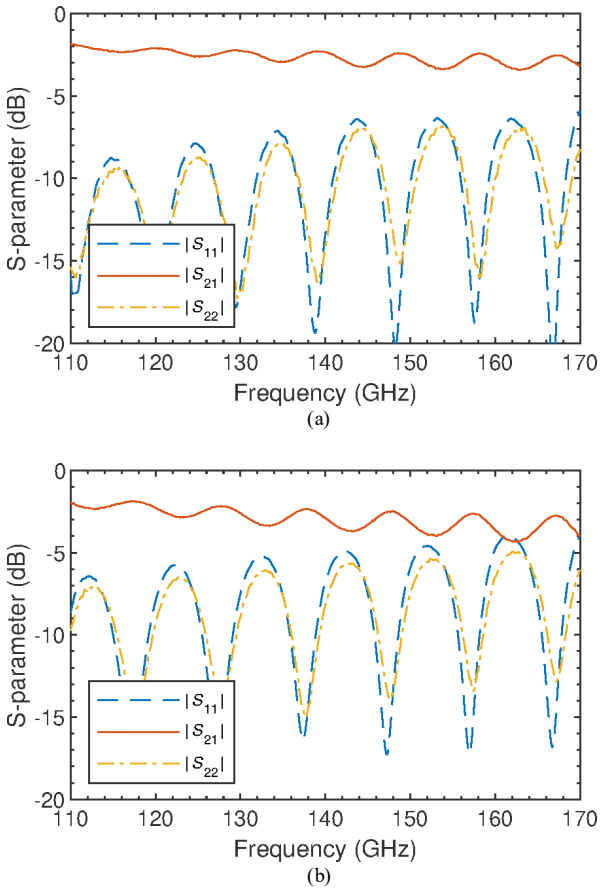

Fig. 8. Measured S-parameters (LRRM calibration) for the 10-mm long (a) microstrip line and (b) coplanar waveguide on PCB using Megtron 7N by Panasonic and the mSAP technology.

To extract the influence of pads from the results, also the thru-reflect-line (TRL) calibration method was used in the measurements. The measured S-parameters for the 10 mm long MS and GCPW are presented in Fig. 9. MS and GCPW losses are 1.9 dB/cm and 1.8 dB/cm at 150 GHz, respectively. After the TRL calibration both MS and GCPW are well matched.

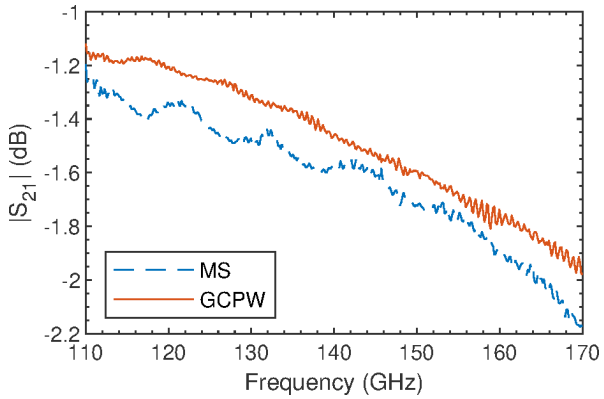

Fig. 9. Measured $|S_{21}|$ (TRL calibration) for the microstrip line and coplanar waveguide on PCB using Megtron 7N by Panasonic and the mSAP technology.

B. Flip chip interconnect

The same test setup and TRL calibration described above are used for performing the measurements of the structures with the flip-chipped chips. Thus, influence of pads are extracted from the results. Due to strong over-etching of subtractive processed PCB only PCB using Megtron 7N by Panasonic as substrate material and semi-additive processing (mSAP) for conductor patterning were utilized for characterization of flip-chip interconnects. Five chips were flip-chipped on the test PCB. Fig. 10 shows the measured $|S_{21}|$ for samples tested. Fig. 11 shows all S-parameters for the best sample. The test results include: 2×1.5 mm PCB line (total loss 0.6 dB), 2× flip-chip transition loss, and the on-chip microstrip line loss (about 1.5 dB). The estimate for a single flip-chip transition loss is about 0.3 dB.

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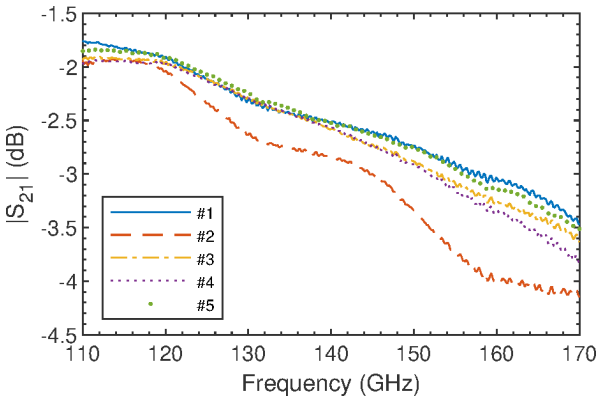

Fig. 10. $|S_{21}|$ results with flip chip bumps (diam. 60 µm) for tested samples on PCB using PCB using Megtron 7N by Panasonic and the mSAP technology

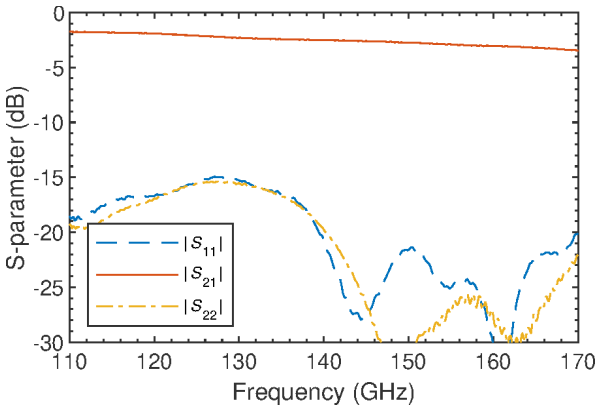

Fig. 11. S-parameters for the best flip chipped sample on PCB using Megtron 7N by Panasonic and the mSAP technology.

IV. Conclusions

The paper presents the characterization results of interconnects for D-band on multilayer high frequency PCBs. Both studied substrate materials (Astra MT77 and Megtron 7N) have demonstrated their applicability for D-band. The measured losses for microstrip line and coplanar waveguide at 150 GHz are 1.9 dB/cm and 1.8 dB/cm, respectively. Such transmission line losses enable the construction of feed networks for antenna arrays with 64-, 256- or 512-elements. The critical areas for fabrication of interconnects are the GSG contact pads needed for flip chip bonding interconnects. Track widths down to 50 µm and gap widths of 50 µm are required for their realization. Utilization of PCB with semi-additive processing (mSAP) for conductor patterning allows reaching such accuracy. The measured performance of a single flip-chip transition loss is about 0.3 dB for 60 µm bumps. The feasibility of PCB technology for a low cost integration platform even at D-band is proven.

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